A SUCCESSFUL AND EASY METHOD TO REMOVE POLYSILICON FILM

FIELD OF THE INVENTION

The present invention relates generally to semiconductor fabrication and more specifically to reworking of semiconductor wafers by removing polysilicon films.

BACKGROUND OF THE INVENTION

Many times wafers must be scrapped if they suffer from thickness abnormally or particle problems after polysilicon deposition.

U.S. Patent No. 5,928,969 to Li et al. describes a method for controlled selective polysilicon etching employing an NH_4OH plus NH_4F polysilicon etch and a hemispherical grain (HSG) polysilicon process.

U.S. Patent Nos. 6,100,203 to Kil et al. describes a polysilicon etch and subsequent aqueous cleaning composition cleaner methods.

U.S. Patent No. 5,431,777 to Austin et al. describes methods and compositions for the selective etching of silicon.

U.S. Patent No. 5,296,093 to Szwejkowdki et al. describes a process for removal of residues remaining after etching a polysilicon layer.

U.S. Patent No. 5,030,590 to Amini et al. describes a process for etching a polysilicon layer in the formation of an integrated circuit structure.

U.S. Patent No. 4,113,551 to Bassous et al. describes a method for polycrystalline silicon etching with tetramethylammonium hydroxide.

U.S. Patent No. 5,963,804 to Figura et al. describes a method of making a doped silicon structure with an impression image on opposing roughened surfaces.

U.S. Patent No. 5,976,767 to Li describes a process for selectively removing silicon containing material using an ammonium hydroxide etch.

SUMMARY OF THE INVENTION

Accordingly, it is an object of an embodiment of the present invention to provide an improved method of selectively removing polysilicon.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a structure having a non-silicon layer formed thereover is provided. A first polysilicon layer is formed upon the non-silicon layer. The first polysilicon layer is removed from over the non-silicon layer to expose the non-silicon layer using a NH_4OH:DIW dip solution process having a NH_4OH:DIW ratio of from about 1:2 to 1:8. Whereby the non-silicon layer is substantially unaffected by the NH_4OH:DIW dip solution process.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 4 schematically illustrate a preferred embodiment of the present invention, with Figs. 2 through 4 being an enlargement of a portion of Fig. 1 designated "Fig. 2" and illustrating the method of the present invention .

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Unless otherwise specified, all structures, layers, steps, methods, etc. may be formed or accomplished by conventional steps or methods known in the prior art.

Initial Structure

Fig. 1 illustrates a dynamic random access memory (DRAM) structure 10 formed on a structure 11. Commonly many such DRAM structures 10 are formed on structure 11 along with other integrated circuit devices (not shown).

Structure 11 is preferably a silicon substrate and is understood to possibly include a semiconductor wafer or substrate, active and passive devices formed within the wafer, conductive layers and dielectric layers (e.g., inter-poly oxide (IPO), intermetal dielectric (IMD), etc.) formed over the wafer surface. The term "semiconductor structure" is meant to include devices formed within a semiconductor wafer and the layers overlying the wafer.

DRAM structure 10 includes a trench 12 lined with a polysilicon (poly) layer 14. Poly layer 14 is preferably from about 400 to 460Å thick, is more preferably from about 415 to 445Å thick and is most preferably about 430Å thick.

Rugged poly nodules 16 are formed over the surface of poly layer 14 within trench 12. An ONO capacitor dielectric layer 18 (not shown in Fig.1 - see Figs. 2 to 4 for a detailed description of the ONO capacitor dielectric layer 18) is formed over the rugged poly nodules 16 and over the surface of poly layer 14.

A poly layer 26 is formed over the ONO capacitor dielectric layer 18 to a thickness of preferably from about 640 to 780Å, more preferably from about 675 to 745Å thick and most preferably about 710Å. It is noted the method of the present invention is not limited to the above thicknesses of the poly layer 26.

Detailed View of Rugged Poly Nodules 16

Fig. 2 is an enlarged portion of Fig. 1 designated "Fig. 2" showing a detailed view of a sample rugged poly nodule 16 and showing, inter alia, the ONO capacitor dielectric layer 18.

As shown in Fig. 2, ONO capacitor dielectric layer 18 is comprised of: an inner silicon oxide (oxide) layer 20 adjacent rugged poly nodules 16 and the surface of poly layer 14; a middle silicon nitride (nitride) layer 22 over the inner oxide layer 20; and an outer oxide layer 24 over the middle nitride layer 22.

Inner oxide layer 20 is preferably from about 10 to 14Å thick, is more preferably from about 11 to 13Å thick and is most preferably about 12Å thick.

Middle nitride layer 22 is preferably from about 39 to 48Å thick, is more preferably from about 41 to 45Å thick and is most preferably about 43Å thick.

Outer oxide layer 24 is preferably from about 22 to 28Å thick, is more preferably from about 24 to 26Å thick and is most preferably about 25Å thick. Outer oxide layer 24 may be comprised of silicon oxide, an ONO composite layer, nitride, TEOS oxide or HTO oxide.

For a variety of reasons, such as, for example, an abnormal thickness or a particle abnormality, the poly layer 26 formed over the ONO capacitor dielectric layer 18 may be found to be defective and would result in an unacceptable failure or poor performance rate of at least the DRAM devices 10. To re-work, or reuse the wafer, the poly layer 26 must be removed and replaced.

Removal of Defective Poly Layer 26 - Key Step of the Invention

As shown if Fig. 3, the defective poly layer 26 is removed from the structure of Fig. 2 without appreciable affecting the outer oxide layer 24 of the ONO capacitor dielectric layer 18.

First, an HF dip is used to remove any native oxide formed on the defective poly layer 26 surface. The HF dip is preferably performed using about a 2.5% HF solution at about 25°C for about 30 seconds.

The structure is then subjected to a five (5) minute deionized water (DIW) rinse.

Then, in a key step of the invention, the defective poly layer 26 is stripped using a NH_4OH:deionized water (DIW) dip at temperature of preferably from about 25 to 60°C, more preferably from about 30 to 50°C and most preferably about 40°C until bubble formation ceases. The bubbles formed are a very small amount of H_2 and has no impact on the fabrication (fab) operation. Visual monitoring of the NH_4OH:DIW dip solution may be used to determine when bubble formation ceases which indicates that the poly layer 26 strip is complete.

The NH_4OH:DIW dip is preferably from about 1:2 to 1:8 NH_4OH:DIW, more preferably from about 1:4 to 1:6 NH_4OH:DIW and most preferably about 1:5 NH_4OH:DIW.

The NH_4OH:DIW dip has a high etch selectivity of poly:oxide so that the outer oxide layer 24 of the ONO capacitor dielectric layer 18 underlying the defective poly layer 26 is substantially unaffected and is not itself partially or completely removed. The poly:oxide selectivity of the NH_4OH:DIW dip is preferably about 680:1, more preferably about 1650:1 and most preferably about 1160:1. The poly etch rate (E/R) is preferably about 560Å/minute, more preferably from about 560Å/minute to 580Å/minute and is most preferably about 580Å/minute.

The use of the NH_4OH:DIW dip of the present invention must be used in the absence of H_2O_2 as the inventor has discovered that even a small amount of H_2O_2 severely impacts the etch selectivity, for example from about 580Å/minute to below about 2Å/minute.

Spiking conditions must also be considered because NH_4OH easily evaporates, especially at high temperature, i.e. above about 40°C. That is , a small amount of NH_4OH is added, or spiked, to the process tank to make up for the evaporated NH_4OH during the processing period.

The inventor has determined that, compared to other poly etch solutions, the NH_4OH:DIW solution of the present invention has a much superior poly:oxide selectivity, for example:

Chemical Solution	Poly E/R (Å/min)	Oxide E/R (Å/min)	Selectivity (Poly:Oxide)
1:5 NH_4OH:DIW	about 580	about 0.5	about 1160
2.5% HF @ 25°C	< about 10	about 160	< about 1
1:1:5 APM @ 40°C	about 0.13	about 0.29	< about 1
155°C H_3PO_4	about 8	< about 1	about 8
M1 ($HF/HNO_3/CH_3COOH$)	about 14,000	about 400	about 35

Where "APM" is ammonia peroxide mixture (NH_4OH/H_2O_2/deionized water (DIW)).

The selectivity for all but the NH_4OH:DIW solution of the present is too low to protect the outer oxide layer 24 during the poly etching and the etch rate for the M1 solution (poly:14,000 Å/minute and oxide: 400 Å/minute), which has a poly:oxide selectivity of 35, is much too great to protect the outer oxide layer 24 during the poly etch.

Further, the inventor has determined that, at about 40°C the selectivity of the NH_4OH:DIW solution of the present invention varies as shown below for changes in the NH_4OH:DIW ratio as shown:

NH_4OH:DIW ratio	1:2	1:5	1:8
Selectivity (Poly/Oxide)	about 1650	about 1160	about 680

Further yet, the inventor has determined that, at about 1:8 NH_4OH:DIW ratio, the selectivity of the NH_4OH:DIW solution of the present invention varies as shown below for the changes in the temperature as shown:

Temperature	25°C	40°C	60°C
Selectivity (Poly/Oxide)	about 320	about 680	about 940

DIW Rinse

The structure of Fig. 3 is then subjected to a DIW rinse lasting for preferably about 5 minutes and the structure is then dried.

Re-Deposition of Polysilicon

As shown in Fig. 4, polysilicon is redeposited over the ONO capacitor dielectric layer 18 to form polysilicon layer 36 having a thickness of preferably from about 640 to 780Å, more preferably from about 675 to 745Å thick and most preferably about 710Å.

Although removing polysilicon from over an ONO layer has been described, the method of the present invention is admirably suited in removing or stripping polysilicon from over other layers except silicon. Such other layers may be comprised of, for example, nitride or metal oxide such as TaO. Nitride layers would be stripped by H_3PO_4 on IC tab, metal oxide layers would be stripped according to their oxide characteristics with TaO layers being stripped of polysilicon using H_2O_2 for example.

Experimental Results

The inventor obtained the following WAT/CP data of reworked runs of wafers designated R 15880.1, R 15906.1 and R 15909.1:

	Capacitor Performance	RSP3NR*	Yield
Spec Low	23	190	
Spec High	45	250	
R 15880.1	32.66	224.68	78.6%
R 15906.1	31.75	183.89	66.9%
R 15909.1**	32.97	220.37	59.9%*

*If poly layer 26 were not completely stripped, the RSP3NR factor (which checks poly resistivity) will show up.
**The R 15909.1 yield of 59.9% was lower due to the fact that 16 wafers suffered low yield while the other wafers were normal. Other factors were suspected to have dominated the lower 59.9% yield apart from the method of the present invention.

With the "Spec Low" and "Spec High" being the required ranges for the indicated parameters.

Advantages of the Present Invention

The advantages of the present invention include:

1. high etch selectivity for polysilicon:non-silicon film;

2. an easy and visible judgement method is provided to confirm process completion;

3. less damage to non-silicon films;

4. low cost process;

5. safety methodology on this procedure; and

6. no extra machine retrofit requirement.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.